REMARKS/ARGUMENT

Claims 15, 18 and 21 have been amended better to overcome the objections to the claims.

1) Claims 1, 3, 5-8, 11, 13-17, 19-22, 24, 27-31, 41, 43, 45 and 46 are stand under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Yamaguchi et al. (US 6,687,629 B1). Applicants respectfully traverse this rejection as set forth below.

Claim 1 requires and positively recites, a method for testing a radio frequency (RF) circuit comprising: "observing a signal from the RF circuit, wherein the signal is a digital signal from within a processing portion of the RF circuit, **wherein the signal has a high degree of correlation with an RF output of the RF circuit**, and **wherein the observing occurs outside of the RF circuit**", "manipulating the signal outside of the RF circuit" and "producing a metric for the test outside of the RF circuit based on results from the manipulating".

Claim 41 requires and positively recites, a circuit comprising: "a reference phase accumulator coupled to a signal input, the reference phase accumulator containing circuitry to compute a reference phase", "a phase detector coupled to the reference phase accumulator, the phase detector containing circuitry to compute a difference between the reference phase and a variable phase", "a digitally-controlled oscillator (DCO) coupled to the phase detector, wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation" and "a variable phase accumulator coupled to the DCO and the phase detector, the variable phase accumulator containing circuitry to compute the variable phase".

In contrast, Girardeau teaches an apparatus and method for determining a feedback divider ratio in a digital phase locked loop (DPLL) by monitoring the drift in the feedback signal. The drift could be caused by using an unknown frequency of fixed frequency system clock 22. (col. 2, lines 28-39). Examiner equates the observed "signal from the RF circuit" to the 1-bit digital signals EARLY 30 and LATE 32 from the phase detector 12 – they are collectively labeled as 104 in the timing diagram in Figure 2. Examiner also equates the Digital Oscillator output 23 with the "RF output of the RF circuit" (in the last office action, label 24 appears to be typo and Applicants take liberty to correct it to 23 as used by the Examiner in the previous office action.)

The EARLY/LATE phase detector output signal in Girardeau does not satisfy Claim 1's limitation "**wherein the signal has a high degree of correlation with an RF output of the RF circuit**". "Signal ... correlation with an RF output", as required by Claim 1, necessitates that the phase detector output correlates with the frequency drift of the oscillator. Such is not the case with Girardeau's oscillator 23. Girardeau's phase detector output is a sign of the phase relationship between the reference oscillation 26 and the feedback oscillation 28 synchronous to the reference oscillation 26 clock. That 1-bit (only early/late information) signal cannot possibly correlate with the frequency deviation of the output of oscillator 23. Reason one; 1-bit of information cannot have a "high degree of correlation" with the frequency drift. Reason two, the 1-bit signal is a sign of phase, which is time integral of frequency, and even the full resolution of the phase error can not be correlated to the frequency drift, without first integrating it. Accordingly, resolution of the phase error and integrating the phase error are not taught in Girardeau since there would be no motivation of doing so.

What makes the DPLL in Girardeau responsive to the frequency drift, which is the premise of Girardeau's invention, is the other mechanism which includes Adjuster 18, Feedback Divider 20, Threshold Unit 21, Second Comparator 14 and Third Comparator 16. Accordingly, Girardeau fails to teach or suggest, "**wherein the signal**

has a high degree of correlation with an RF output of the RF circuit", as required by Claim 1.

In addition to the above difference between Girardeau and Claim 1, Examiner admits that Girardeau does not teach or suggest, "**wherein the observing occurs outside of the RF circuit**", as further required by Claim 1. Examiner offers Yamaguchi as teaching this limitation not disclosed in Giradeau. Yamaguchi shows in Figure 29 a spectrum analyzer connected to the output of a "phase detector." This example, however, is irrelevant to the claimed invention for the following reasons:

1. Yamaguchi teaches measuring jitter of an **external** clock connected to Phase Detector **that forms a PLL loop** together with Signal Generator to generate the other Phase Detector input ("A clock signal under test is inputted to a phase detector as a reference frequency." col. 15, lines 30-32; and "In this case, the phase detector and the signal generator compose a phase-locked loop." col. 15, lines 32-33). This teaching in Yamaguchi clearly states that the phase detector itself would be useless since the other phase detector input (non-"reference" or variable) needs to be created as well as a means to perform phase locking to the "reference" input.

2. The above requirement to form a PLL loop with the Phase Detector stems from the fact that Yamaguchi teaches measuring jitter of an **external** clock. In contrast, the present invention does not concern itself with measuring performance of some external, unrelated clock. Rather, it deals with measuring performance of a signal generated by the RF circuit by observing and manipulating signals from within the RF circuit. In the embodiment examples in Figures 2 (frequency synthesizer) and 3 (frequency synthesizer-based transmitter) of the instant application, the PLL is part of the RF circuit itself. The performance of these RF circuits does not simply depend on one clock – it is a combination of the reference clock, variable clock generated by the DCO within the RF circuit, as well as the PLL loop parameter settings.

3. "An RMS jitter JRMS of a clock signal is measured in **frequency domain.**" (col. 15, lines 27-28). In contrast, the present invention operates in the time domain and does not need to resort to operating in the frequency domain.

These differences are significant and make it clear why Yamaguchi cannot be simply incorporated into Girardeau to form the prior art. As a result, any combination of Girardeau and Yamaguchi fails to teach or suggest, "observing a signal from the RF circuit, wherein the signal is a digital signal from within a processing portion of the RF circuit, **wherein the signal has a high degree of correlation with an RF output of the RF circuit,** and **wherein the observing occurs outside of the RF circuit**", as required by Claim 1. Accordingly, the 35 U.S.C. 103(a) rejection of Claim 1 is improper and must be withdrawn.

Applicants respectfully point out that, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Moreover, even had the Examiner considered all of the words of Claim 1, in proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** *In re Gordon*, 733 F.2d at 902, 221

USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Claims 3, 5-8, 11, 13-17, 19-22, 24 and 27-31 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 3 further defines the method of claim 1, **wherein the signal is a phase error signal.** Claim 3 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Further, Girardeau shows in Figure 1 a digital phase locked loop (DPLL), which comprises a phase detector 12 that produces two 1-bit digital signals EARLY 30 and LATE 32, which the Examiner improperly equates to the phase error. These signals are a very crude representation of the phase relationship between the reference oscillation 26 and feedback oscillation 28 and only indicate which phase detector input is ahead of the other with no information of how much (col. 2, lines 50-61). Thus, only the sign of the phase error is produced with the actual magnitude or value missing. The EARLY and LATE signals cannot be equated with the phase error of the instant application, which has information of the actual phase error value.

If, arguendo, the EARLY 30 and LATE 32 output of the phase detector were to be equated with the phase error, observing and manipulating the phase error sign signal with the magnitude part missing would not be useful. Accordingly, Girardeau in combination with Yamaguchi does not teach or suggest "wherein the signal is a phase error signal". The 35 U.S.C. 103(a) rejection of Claim 3 is improper and must be withdrawn.

Claim 4 is canceled. Accordingly, the 35 U.S.C. 103(a) rejection is moot.

Claim 5 further defines the method of claim 3, wherein a transfer function between the signal and the RF output phase is flat within a frequency band of interest. Claim 5 is allowable for the same reasons set forth above in support of the allowance of Claim 3. Moreover, being there is no correlation in Girardeau between the 1-bit phase detector 12 output 30/32 with the frequency drift of the oscillator 23, the discussion of the transfer function flatness is irrelevant. If, arguendo, the phase detector would produce full resolution phase error and the system somehow made to work, then, the transfer function would not be flat as a result of the frequency being the time derivative of phase.

Moreover, Applicants traverse Examiner's determination, "when the PLL is in a lock mode the output signal and **the input signal** are the same, thus, exhibiting a transfer function which is flat." Examiner's use of the input signal instead of the "signal from the RF circuit" to analyze the transfer function is impermissible since it has nothing to do with the wording of claim 5 and is not relevant to the technical feasibility of the claim.

Claim 6 further defines the method of claim 1, wherein the RF circuit is an all-digital circuit, and wherein the signal is an output of a component in an all-digital phase-locked loop in the RF circuit. Claim 6 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 7 further defines the method of claim 6, wherein the signal is an output of a phase detector. Claim 7 is allowable for the same reasons set forth above in support of the allowance of Claim 6.

Claim 8 further defines the method of claim 7, wherein the signal has been filtered. Claim 8 is allowable for the same reasons set forth above in support of the allowance of Claim 7.

Claim 11 further defines the method of claim 8, wherein a loop filter coupled to an output of a phase detector performs the filtering, and wherein the signal is an output of the loop filter. Claim 11 is allowable for the same reasons set forth above in support of the allowance of Claim 8.

Claim 13 further defines the method of claim 1, wherein the frequency of the signal is several orders of magnitude less than the frequency of the RF output. Claim 13 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 14 further defines the method of claim 1, wherein the test is for phase error trajectory and the signal is the output of a phase detector, and wherein the manipulation comprises measuring a change in the signal. Claim 14 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 15 further defines the method of claim 14, wherein the phase error trajectory is good when the change in the signal is less than a specified threshold. Claim 15 is allowable for the same reasons set forth above in support of the allowance of Claim 14.

Claim 16 further defines the method of claim 14, wherein the measuring the change in the signal comprises measuring a peak, a variance, or a rate of change in the signal. Claim 16 is allowable for the same reasons set forth above in support of the allowance of Claim 14.

Claim 17 further defines the method of claim 1, wherein the test is for frequency lock and the signal is the output of a phase detector, and wherein the manipulation comprises comparing a value of the signal over several samples. Claim 17 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 19 further defines the method of claim 17, wherein the samples are taken at different times. Claim 19 is allowable for the same reasons set forth above in support of the allowance of Claim 17.

Claim 20 further defines the method of claim 1, wherein the test is for frequency deviation and the signal is an output of an integral accumulator of a loop filter, and wherein the manipulation comprises comparing the signal with a specified range. Claim 20 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 21 further defines the method of claim 20, wherein the frequency deviation is within acceptable limits when the signal is within the specified range. Claim 21 is allowable for the same reasons set forth above in support of the allowance of Claim 20.

Claim 22 further defines the method of claim 20, wherein the manipulation further comprises comparing several samples of the signal. Claim 22 is allowable for the same reasons set forth above in support of the allowance of Claim 20.

Claim 24 further defines the method of claim 1, wherein the RF circuit contains an all-digital phase-locked loop, and the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth. Claim 24 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 27 further defines the method of claim 1, wherein the RF circuit is an all-digital frequency synthesizer. Claim 27 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 28 further defines the method of claim 1, wherein the RF circuit is an all-digital transmitter. Claim 28 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 29 further defines the method of claim 28, wherein the transmitter is used in a wireless communications network. Claim 29 is allowable for the same reasons set forth above in support of the allowance of Claim 28.

Claim 30 further defines the method of claim 29, wherein the wireless communications network is Bluetooth compliant. Claim 30 is allowable for the same reasons set forth above in support of the allowance of Claim 29.

Claim 31 further defines the method of claim 1, wherein the testing comprises a functional test or a compliance test of the RF circuit. Claim 31 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 41 requires and positively recites, a circuit comprising: "a **reference phase accumulator** coupled to a signal input, the reference phase accumulator containing circuitry to compute a reference phase", "a phase detector coupled to the reference phase accumulator, the phase detector containing circuitry to compute a difference between the reference phase and a variable phase", "a **digitally-controlled oscillator (DCO)** coupled to the phase detector, wherein the performance of the DCO can be ascertained by a test circuit outside of the circuit observing an output of the phase detector, wherein

the test circuit manipulates the observed output and generates a performance metric for the DCO based, at least in part, on the manipulation" and "a **variable phase accumulator** coupled to the DCO and the phase detector, the variable phase accumulator containing circuitry to compute the variable phase".

Applicants respectfully traverse Examiner's determination (pp. 11 of the office action) that "Claim 41 is a system claim corresponding to method claim 1" and further determination that "Hence, the steps performed in method claim 1 would have necessitated the elements in system claim 41." Claim 41 is an apparatus claim that contains limitations obviously not present in method claim 1, including: "**reference phase accumulator**", "**digitally controlled oscillator**" and "**variable phase accumulator**". Applicants respectfully point out that, "all words in a claim must be considered in judging the patentability of that claim against the prior art." In re Wilson, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970). The above clearly shows that Examiner did not consider all of the limitations of Claim 41. Accordingly, the 35 U.S.C. 103(a) is improper and must be withdrawn. Further, even were the rejection to not be improper on its face, Claim 41 would be allowable for similar reasons as those set forth in the allowability of Claim 1. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claims 43, 45 and 46 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 43 further defines the circuit of claim 41 further comprising a loop filter coupled to the phase detector and the DCO, the loop filter to provide a desired amount

of attenuation to the computed difference between the reference phase and the variable phase. Claim 43 is allowable for the same reasons set forth above in support of the allowance of Claim 41. Moreover, Examiner's proposed combination would not possibly work as suggested. First of all, the analog loop filter in Yamaguchi cannot be possibly combined with the 1-bit digital signals in Girardeau. Even if the 1-bit digital signals were to be converted to analog and then to digital through D/A and A/D converter, respectively, the system would fail to properly operate. Second, even if, arguendo, the signals were digital, it is not obvious how the filtering should be performed on the 1-bit EARLY & LATE signals in a way as to "to provide a desired amount of attenuation to the computed" and still produce the 1-bit RETARD & ADVANCE input signal to the Digital Oscillator 23. Examiner's determination seems to be supposition not supported by fact since Examiner does not offer any explanation or further details. Consequently, the combining of references as suggested by the Examiner would not work and the claim rejection is improper.

Claim 45 further defines the circuit of claim 44, wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a parallel fashion. Claim 45 is allowable for the same reasons set forth above in support of the allowance of Claim 44. Further, Examiner has provided no reasoning for the rejection of this claim. Accordingly, no prima facie case of obviousness of claim 45 has been established. The 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 46 further defines the circuit of claim 44, wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a cascaded fashion. Claim 46 is allowable for the same reasons set forth above in support of the allowance of Claim 44. Further, Examiner has provided no reasoning for the rejection of this claim. Accordingly, no prima facie case of

obviousness of claim 46 has been established. The 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

2) Claim 24 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Yamaguchi et al. (US 6,687,629 B1), as applied to claim 1 above, and further in view of Skierszkan et al. (US Publication 2002/0001359 A1). Applicants respectfully traverse this rejection as set forth below.

Claim 24 further defines the method of claim 1, wherein the RF circuit contains an all-digital phase-locked loop, and the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth. Claim 24 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Moreover, Applicants respectfully traverse Examiner's determination: "Skierszkan discloses an acquisition PLL that has a low pass filter with a relatively high cut-off frequency. The acquisition PLL tracks all changes in the input signal, including error components." In actuality, the "acquisition PLL" is a separate PLL and adding a new PLL to the DPLL in Girardeau would not work since having two PLL's would bring issues of their differing performances, such as jitter or drift. The two PLL's would have separate oscillators and each oscillator is independent. Since the topic of Girardeau's invention is testing, now Girardeau's tests would need to be duplicated without solving the fundamental issue of setting *the* PLL into different bandwidth. Accordingly, Examiner's combination of Girardeau, Yamaguchi and Skierszkan and corresponding rejection of Claim 24 is improper and must be withdrawn.

3) Claim 45 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Yamaguchi et al. (US 6,687,629 B1), as

✓

applied to claims 1 and 45 above, and further in view of Ko et al. (US 5,982,832). Applicants respectfully traverse this rejection as set forth below.

Claim 45 further defines the circuit of claim 44, wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a parallel fashion. Claim 45 is allowable for the same reasons set forth above in support of the allowance of Claim 44. Moreover, Figure 4 in Ko does not show "a plurality of filters arranged in a parallel fashion", as suggested by Examiner. The cited text describes the structure filters as n filters with the phase detector selecting one filter among the n filters. In addition, combining Ko into Girardeau would not work since the output of such a filer could not be connected to the oscillator 23. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

4) Claim 46 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Yamaguchi et al. (US 6,687,629 B1), as applied to claims 1 and 41 above, and further in view of Cucchietti et al. (US 4,819,080). Applicants respectfully traverse this rejection as set forth below.

Claim 46 further defines the circuit of claim 44, wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a cascaded fashion. Claim 45 is allowable for the same reasons set forth above in support of the allowance of Claim 44. Moreover, Combining Cucchiett into Girardeau would not work since the output of such a filer could not be connected to the oscillator 23. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

5) Claim 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Yamaguchi et al. (US 6,687,629 B1), as applied

to claim 1 above, and further in view of Kim et al. (US 6,885,700). Applicants respectfully traverse this rejection as set forth below.

Claim 2 further defines the method of claim 1, wherein the testing is performed using built-in self test (BIST) techniques. Claim 45 is allowable for the same reasons set forth above in support of the allowance of Claim 44. Furthermore, the combination of Girardeau, Yamaguchi and Kim does not satisfy the limitation "wherein the **testing** is performed", which is positively recited and required by Claim 2. Girardeau does not teach or even suggest testing and incorporating Yamaguchi and Kim will change nothing in this regard.

Combining Kim into Girardeau does not make sense because the objective of the DPLL in Girardeau is not test or even built-in self-test (BIST) but the main or mission mode of its operation, which includes agility and being robust over the changing environment. Girardeau teaches an apparatus and method for determining a feedback divider ratio in a digital phase locked loop (DPLL) by monitoring the drift in the feedback signal. The drift could be caused by using an unknown frequency of fixed frequency system clock 22. (col. 2, lines 28-39). Hence monitoring the frequency drift of the external clock is not related to testing, so there is no motivation to incorporate Kim. Furthermore, the test or BIST would imply reporting back the results outside of the circuit. No such mechanism is reported in Girardeau simply because he does not teach the test or BIST. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

6) Claims 10 & 44 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Yamaguchi et al. (US 6,687,629 B1), as applied to claim 1 above, and further in view of Mathe et al. (US 5,825,253). Applicants respectfully traverse this rejection as set forth below.

Claim 10 further defines the method of claim 8, wherein the all-digital phase-lock loop is operating in a type-I mode, and the signal is an output of an infinite impulse response filter coupled to the output of a loop filter. Claim 10 is allowable for the same reasons set forth above in support of the allowance of Claim 8. Further, Mathe cannot be combined with Girardeau since operating on a 1-bit output of the phase detector by an IIR filter would change the signal nature (i.e., multi-bit) which will make the DPLL system inoperable. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 44 further defines the circuit of claim 43, wherein the loop filter is of a type selected from a group consisting of a finite impulse response filter, an infinite impulse response filter or combination thereof. Claim 44 is allowable for the same reasons set forth above in support of the allowance of Claim 43. Further, Mathe cannot be combined with Girardeau since operating on a 1-bit output of the phase detector by an FIR filter or IIR filter or a combination thereof would change the signal nature (i.e., multi-bit), which would not connect to the oscillator 23 (requires 1-bit RETARD/ADVANCE signals) and which will further make the DPLL system inoperable. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

7) Claims 12 & 47 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Yamaguchi et al. (US 6,687,629 B1), as applied to claims 1 and 41 above, and further in view of Koshiro et al. (US 5,768,326). Applicants respectfully traverse this rejection as set forth below.

Claim 12 further defines the method of claim 6, wherein the signal is an output of a gain normalization block. Claim 12 is allowable for the same reasons set forth above in support of the allowance of Claim 6. Moreover, it is not possible to normalize

the 1-bit output of the phase detector 30/32, which is equated by the Examiner to "signal" in the present claim. Consequently, incorporating Koshiro into Girardeau does not make sense and would not possibly work.

Further, even if, arguendo, it were possible in Girardeau to normalize the phase detector output, doing so would not make much sense. The Digital Oscillator 23 is a purely digital circuit ("comprises a counter and a decoder"; col. 3, line 17) synchronously operating on Unknown System Clock 22 so its gain is known precisely. In contrast, the oscillator characteristics in the instant application are subject to process, voltage and temperature variations so normalizing the signal to the gain of the oscillator is beneficial. No such motivation exists in Girardeau. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 47 further defines the circuit of claim 41 further comprising a gain normalization unit coupled to the phase detector and the DCO, the gain normalization unit to normalize the difference between the reference phase and the variable phase with respect to a gain in the DCO. Claim 47 is allowable for the same reasons set forth above in support of the allowance of Claim 41. Moreover, it is not possible to normalize the 1-bit output of the phase detector 30/32, which is equated by the Examiner to "signal" in the present claim. Consequently, incorporating Koshiro into Girardeau does not make sense and would not possibly work.

Further, even if, arguendo, it were possible in Girardeau to normalize the phase detector output, doing so would not make much sense. The Digital Oscillator 23 is a purely digital circuit ("comprises a counter and a decoder"; col. 3, line 17) synchronously operating on Unknown System Clock 22 so its gain is known precisely. In contrast, the oscillator characteristics in the instant application are subject to process, voltage and temperature variations so normalizing the signal to the gain of the oscillator

is beneficial. No such motivation exists in Girardeau. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

8) Claim 18 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Yamaguchi et al. (US 6,687,629 B1), as applied to claims 1 and 41 above, and further in view of Gustafson et al. (US 4,086,539). Applicants respectfully traverse this rejection as set forth below.

Claim 18 further defines the method of claim 17, wherein the frequency has been locked when a variance in the magnitude is less than a specified threshold. Claim 18 is allowable for the same reasons set forth above in support of the allowance of Claim 17. Further, it is not possible to compute variance of the 1-bit phase detector output in Girardeau. The phase detector output is a sign signal so computing variance of a sign would be meaningless. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

9) Claim 42 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Yamaguchi et al. (US 6,687,629 B1), as applied to claim 41 above, and further in view of Knudsen et al. (US 7,079,611). Applicants respectfully traverse this rejection as set forth below.

Claim 42 further defines the circuit of claim 41 further comprising a time-to-digital converter (TDC) coupled to the DCO and the phase detector, the TDC containing circuitry to compute a time difference between a reference clock and a variable clock. Claim 42 is allowable for the same reasons set forth above in support of the allowance of Claim 41. Further, adding the teachings of Knudsen, which introduces a circuit to compute and digitize a time difference between clocks, to Girardeau does not seem to

make any sense. Claim 42 is a dependent claim of Claim 41, not Claim 1. The Examiner has not shown how other elements of Claim 41 are equated with Girardeau. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

10) Claims 32, 34 and 36-40 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (US 5,295,079). Applicants respectfully traverse this rejection as set forth below.

Independent Claim 32 requires and positively recites, a circuit comprising: "a processor coupled to a radio frequency (RF) circuit, the processor containing circuitry to manipulate digital signals from the RF circuit to provide a performance metric for the RF circuit" and "**a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals**".

In contrast, Wong describes a phase locked loop (PLL) nominally operating at 125 MHz for clock recovery of a 125 Mbits/s FDDI data. The PLL contains access ports connected to an I/O controller that interfaces with an external Tester 4. The PLL consists of a Phase Detector 10, Phase Error Processor (PEP) 12 performing phase error decimation and quantization and outputting 1-bit digital signal carrying UP/DOWN and Data_valid flag, Loop Filter 14 controlled by Loop Configuration Port (LCP) 24, Phase-to-Frequency Converter (PFC) 16 to generate a triangular wave of controllable frequency, and a Frequency Controlled Oscillator (FCO) 18. The FCO operates at two times the output frequency and is fed by equally-spaced 250 MHz clock and is followed by a divide-by-two 20 circuit. The loop filter integral signal couples with Frequency Access Port (FAP) 26. The accumulated ("sawtooth patterns") up/down bits are coupled with the Phase Access Port (PAP) 28. The PEP outputs are decimated by 44, so its output data rate as well as any other 'down-stream' circuit until the FCO is

125Mbps/44=2.84Mbps. The I/O controller link 6 connects the tester 4 with the LCP 24, FAP 26 and PAP 28.

Wong's system is engineered in such as way as to minimize the data rate accessible through the I/O controller. Hence, the phase detector 10 output is not accessible nor is the PEP 12 output – making them available (despite various technical difficulties) would not provide any substantial benefits. For the above reasons, Wong does not teach or suggest, "**a control signal input coupled to the processor, wherein the control signal input can enable an observation and manipulation of the digital signals.**" The interface in Wong is asynchronous and there is simply no motivation to re-engineer the entire architecture, which in itself is non-obvious to one of average skill in the art at the time of the invention, to allow synchronous signal controls of sufficient speed, as suggested by Examiner. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claims 34 and 36-40 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 34 further defines the circuit of claim 32, wherein the RF circuit is integrated onto a first integrated circuit, wherein the processor is integrated onto a second integrated circuit. Claim 34 is allowable for the same reasons set forth above in support of the allowance of Claim 32.

Claim 36 further defines the circuit of claim 32, wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector. Claim 36 is allowable for the same reasons set forth above in support of the allowance of Claim 32. Furthermore, Examiner is not correct in asserting that the processor in Wong "is coupled to an output of a phase detector". The tester 4, equated

by Examiner to the processor, is coupled only to LCP, FAP and PAP, with FAP being the closest to the output of the phase detector. The phase detector 10 output contains information of the phase error, which is the phase difference between the Din and P_CLK inputs to the phase detector. FAP 26 register, on the other hand, contains "the frequency difference between Din and the local clock generated by the local crystal" (col. 4, lines 60-62) – this is definitely not the phase error. Hence, the tester 4 is not coupled to the phase detector. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 37 further defines the circuit of claim 32, wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to a filtered output of a phase detector. Claim 37 is allowable for the same reasons set forth above in support of the allowance of Claim 32.

Claim 38 further defines the circuit of claim 32, wherein the RF circuit contains an all-digital phase-locked loop, and wherein the processor is coupled to an output of a phase detector and a filtered output of a phase detector. Claim 38 is allowable for the same reasons set forth above in support of the allowance of Claim 32. Furthermore, Examiner is not correct in asserting that the processor in Wong "is coupled to an output of a phase detector". The tester 4, equated by Examiner to the processor, is coupled only to LCP, FAP and PAP, with FAP being the closest to the output of the phase detector. The phase detector 10 output contains information of the phase error, which is the phase difference between the Din and P_CLK inputs to the phase detector. FAP 26 register, on the other hand, contains "the frequency difference between Din and the local clock generated by the local crystal" (col. 4, lines 60-62) – this is definitely not the phase error. Hence, the tester 4 is not coupled to the phase detector. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 39 further defines the circuit of claim 32, wherein the circuit permits the testing of the RF circuit in wafer, in packaged integrated circuit, in factory, and in field. Claim 39 is allowable for the same reasons set forth above in support of the allowance of Claim 32. Moreover, the cited text by Examiner does not show any teaching from Wong "**wherein the circuit permits the testing of the RF circuit in wafer**". The circuit in Wong does not have the inventive features of the present invention to be testable on wafer. The link controller makes it simply unfeasible to reliably connect all the I/O signals between the circuit on wafer and the external tester.

Indeed, the cited text by Examiner does not show any teaching from Wong "**wherein the circuit permits the testing of the RF circuit in field**". The present invention relates to testing of large-scale RF wireless ICs. As it is stated in Background ([0008]), connection to the external test equipment would not feasible after the IC leaves the factory. Such is certainly the case with billions of cellular (GSM) and Bluetooth products in consumer hands at the time of the instant application. Consequently, "in field" would invalidate access to the tester 4 through link 6 in Wong. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 40 further defines the circuit of claim 32, wherein the circuit permits the testing of the RF circuit, and wherein the testing is of a type selected from a group consisting of a phase trajectory error, a frequency lock, a frequency deviation, a phase noise power, or combinations thereof. Claim 40 is allowable for the same reasons set forth above in support of the allowance of Claim 32. Further, as stated already in other places, Wong does not teach or suggests testing of "phase trajectory error" since there is no frequency modulation capability. Similarly, Wong does not teach or suggests testing of "phase noise power". Measuring of a peak jitter does not help with estimating the phase noise power. The instant application describes a method for estimating the phase noise power in paragraph [0058] and in Figure 9d. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

11) Claims 33 & 35 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Wong et al. (US 5,295,079). Applicants respectfully traverse this rejection as set forth below.

Claim 33 further defines the circuit of claim 32 further comprising a latch coupled to the processor, the latch to store the performance metric provided by the processor. Claim 33 is allowable for the same reasons set forth above in support of the allowance of Claim 32.

Claim 35 further defines the circuit of claim 34, wherein the first and the second integrated circuits are the same integrated circuit. Claim 35 is allowable for the same reasons set forth above in support of the allowance of Claim 34.

12) Claims 1, 3, 5-8, 11, 13-17, 19-22, 24, 27-31, 41, 43, 45 and 46 are stand under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Yamaguchi et al. (US 6,687,629 B1). Applicants respectfully traverse this rejection as set forth below.

Claim 1 requires and positively recites, a method for testing a radio frequency (RF) circuit comprising: "observing a signal from the RF circuit, wherein the signal is a digital signal from within a processing portion of the RF circuit, **wherein the signal has a high degree of correlation with an RF output of the RF circuit**, and **wherein the observing occurs outside of the RF circuit", "manipulating the signal outside of the RF circuit"** and "producing a metric for the test outside of the RF circuit based on results from the manipulating".

Claim 41 requires and positively recites, a circuit comprising: "a reference phase accumulator coupled to a signal input, the reference phase accumulator containing circuitry to compute a reference phase", "a phase detector coupled to the reference phase accumulator, the phase detector containing circuitry to compute a difference between the reference phase and a variable phase", "a digitally-controlled oscillator (DCO) coupled to the phase detector, wherein the performance of the DCO can be ascertained by **a test circuit outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO** based, at least in part, on the manipulation" and "a variable phase accumulator coupled to the DCO and the phase detector, the variable phase accumulator containing circuitry to compute the variable phase".

In contrast, Girardeau teaches an apparatus and method for determining a feedback divider ratio in a digital phase locked loop (DPLL) by monitoring the drift in the feedback signal. The drift could be caused by using an unknown frequency of fixed frequency system clock 22. (col. 2, lines 28-39). Examiner equates the observed "signal from the RF circuit" to the 1-bit digital signals EARLY 30 and LATE 32 from the phase detector 12 – they are collectively labeled as 104 in the timing diagram in Figure 2. Examiner also equates the Digital Oscillator output 23 with the "RF output of the RF circuit" (in the last office action, label 24 appears to be typo and Applicants take liberty to correct it to 23 as used by the Examiner in the previous office action.)

The EARLY/LATE phase detector output signal in Girardeau does not satisfy Claim 1's limitation "**wherein the signal has a high degree of correlation with an RF output of the RF circuit**". "Signal ... correlation with an RF output", as required by Claim 1, necessitates that the phase detector output correlates with the frequency drift of the oscillator. Such is not the case with Girardeau's oscillator 23. Girardeau's phase detector output is a sign of the phase relationship between the reference oscillation 26 and the feedback oscillation 28 synchronous to the reference oscillation 26 clock. That

1-bit (only early/late information) signal cannot possibly correlate with the frequency deviation of the output of oscillator 23. Reason one; 1-bit of information cannot have a "high degree of correlation" with the frequency drift. Reason two, the 1-bit signal is a sign of phase, which is time integral of frequency, and even the full resolution of the phase error can not be correlated to the frequency drift, without first integrating it. Accordingly, resolution of the phase error and integrating the phase error are not taught in Girardeau since there would be no motivation of doing so.

What makes the DPLL in Girardeau responsive to the frequency drift, which is the premise of Girardeau's invention, is the other mechanism which includes Adjuster 18, Feedback Divider 20, Threshold Unit 21, Second Comparator 14 and Third Comparator 16. Accordingly, Girardeau fails to teach or suggest, "**wherein the signal has a high degree of correlation with an RF output of the RF circuit**", as required by Claim 1 OR "a digitally-controlled oscillator (DCO) coupled to the phase detector, wherein the performance of the DCO can be ascertained by **a test circuit outside of the circuit observing an output of the phase detector** ...", as required by Claim 41. Examiner admits on page 23 of the Office Action dated 12/12/2007 that Girardeau fails to teach or suggest the above limitation

In addition to the above, Examiner further admits that Girardeau fails to teach or suggest, "manipulating the signal outside of the RF circuit" and "producing a metric for the test outside of the RF circuit based on results from the manipulating" (page 23 of the Office Action dated 12/12/2007). Examiner, however, offers Wong as teaching the above steps missing from Girardeau.

Examiner states:

> The reference of Wong does teach <to enhance accuracy, the digital tester 4 averages several readings of FAP 26. Based on the average reading of FAP 26, the digital tester 4 calculates the expected output frequency (fm) of the PFC 16>. (See col. 4, lines 59-65) By averaging

> several readings of FAP, the tester is somehow manipulating data from the PLL."

Examiner's statement, however, does not establish "**manipulating the signal outside of the RF circuit**", as positively recited and required by Claim 1, OR "… wherein the performance of the DCO can be ascertained by **a test circuit outside of the circuit observing an output of the phase detector, wherein the test circuit manipulates the observed output and generates a performance metric for the DCO** based, at least in part, on the manipulation", as required by Claim 41. Wong only shows that some <u>unrelated signal</u> is being manipulated by an external tester. Previously, Examiner equated the "signal" to the phase detector output 30/32 or 104 in Girardeau. Now, Examiner alleges that Wong teaches that the 1-bit signal 104 could be accessed by the external digital tester 4 in a similar way as the FAP 26 could be read. This combination will not work. The 1-bit signal 104 contains its information not only in the binary value (i.e., early/late) but also in its time position (e.g., see Figure 2: in relation with 106 and 108). Transporting the 104 signal across the asynchronous and lower-speed IO controller 22 and Link 6 in Wong would destroy its time position information, thus making the circuit inoperable. Hence, it is not possible to combine Wong with Girardeau in the manner suggested by Examiner in order to obviate the above claim limitations. Accordingly, no prima facie case of obviousness has been established for Claims 1 and 41. The 35 U.S.C. 103(a) rejection of Claims 1 and 41 is improper and must be withdrawn.

Applicants respectfully point out that, "all words in a claim must be considered in judging the patentability of that claim against the prior art." <u>In re Wilson</u>, 424 F.2d 1382, 1385, 165 USPQ 494, 496 (CCPA 1970).

Moreover, even had the Examiner considered all of the words of Claim 1, in proceedings before the Patent and Trademark Office, "the Examiner bears the burden of establishing a prima facie case of obviousness based upon the prior art". *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992) (citing *In re Piasecki*, 745 F.2d 1468, 1471-72, 223 USPQ 785, 787-88 (Fed. Cir. 1984). "The Examiner can satisfy this burden **only by showing some objective teaching in the prior art or that knowledge generally available to one of ordinary skill in the art would lead that individual to combine the relevant teachings of the references**", *In re Fritch*, 23 USPQ2d 1780, 1783 (Fed. Cir. 1992)(citing *In re Fine*, 837 F.2d 1071, 1074, 5 USPQ2d 1596, 1598 (Fed. Cir. 1988)(citing *In re Lalu*, 747 F.2d 703, 705, 223 USPQ 1257, 1258 (Fed. Cir. 1988)).

Although couched in terms of combining teachings found in the prior art, the same inquiry must be carried out in the context of a purported obvious "modification" of the prior art. **The mere fact that the prior art may be modified in the manner suggested by the Examiner does not make the modification obvious unless the prior art suggested the desirability of the modification.** *In re Gordon*, 733 F.2d at 902, 221 USPQ at 1127. Moreover, **it is impermissible to use the claimed invention as an instruction manual or "template" to piece together the teachings of the prior art so that the claimed invention is rendered obvious.** *In re Gorman*, 933 F.2d 982, 987, 18 USPQ2d 1885, 1888 (Fed.Cir.1991). See also *Interconnect Planning Corp. v. Feil*, 774 F.2d 1132, 1138, 227 USPQ 543, 547 (Fed.Cir.1985).

Claims 3, 5-8, 11, 13-17, 19-22, 24, 27-31, 43 and 45-46 stand allowable as depending from allowable claims and including further limitations not taught or suggested by the references of record.

Claim 3 further defines the method of claim 1, **wherein the signal is a phase error signal**. Claim 3 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Further, Girardeau shows in Figure 1 a digital phase locked loop

(DPLL), which comprises a phase detector 12 that produces two 1-bit digital signals EARLY 30 and LATE 32, which the Examiner improperly equates to the phase error. These signals are a very crude representation of the phase relationship between the reference oscillation 26 and feedback oscillation 28 and only indicate which phase detector input is ahead of the other with no information of how much (col. 2, lines 50-61). Thus, only the sign of the phase error is produced with the actual magnitude or value missing. The EARLY and LATE signals cannot be equated with the phase error of the instant application, which has information of the actual phase error value.

If, arguendo, the EARLY 30 and LATE 32 output of the phase detector were to be equated with the phase error, observing and manipulating the phase error sign signal with the magnitude part missing would not be useful. Accordingly, Girardeau in combination with Wong does not teach or suggest "wherein the signal is a phase error signal". The 35 U.S.C. 103(a) rejection of Claim 3 is improper and must be withdrawn.

Claim 4 is canceled. Accordingly, the 35 U.S.C. 103(a) rejection is moot.

Claim 5 further defines the method of claim 3, wherein a transfer function between the signal and the RF output phase is flat within a frequency band of interest. Claim 5 is allowable for the same reasons set forth above in support of the allowance of Claim 3. Moreover, being there is no correlation in Girardeau between the 1-bit phase detector 12 output 30/32 with the frequency drift of the oscillator 23, the discussion of the transfer function flatness is irrelevant. If, arguendo, the phase detector would produce full resolution phase error and the system somehow made to work, then, the transfer function would not be flat as a result of the frequency being the time derivative of phase.

Moreover, Applicants traverse Examiner's determination, "when the PLL is in a lock mode the output signal and **the input signal** are the same, thus, exhibiting a

transfer function which is flat." Examiner's use of the input signal instead of the "signal from the RF circuit" to analyze the transfer function makes no technical sense.

Claim 6 further defines the method of claim 1, wherein the RF circuit is an all-digital circuit, and wherein the signal is an output of a component in an all-digital phase-locked loop in the RF circuit. Claim 6 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 7 further defines the method of claim 6, wherein the signal is an output of a phase detector. Claim 7 is allowable for the same reasons set forth above in support of the allowance of Claim 6.

Claim 8 further defines the method of claim 7, wherein the signal has been filtered. Claim 8 is allowable for the same reasons set forth above in support of the allowance of Claim 7.

Claim 11 further defines the method of claim 8, wherein a loop filter coupled to an output of a phase detector performs the filtering, and wherein the signal is an output of the loop filter. Claim 11 is allowable for the same reasons set forth above in support of the allowance of Claim 8.

Claim 13 further defines the method of claim 1, wherein the frequency of the signal is several orders of magnitude less than the frequency of the RF output. Claim 13 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 14 further defines the method of claim 1, wherein the test is for phase error trajectory and the signal is the output of a phase detector, and wherein the manipulation comprises measuring a change in the signal. Claim 14 is allowable for the

same reasons set forth above in support of the allowance of Claim 1. Moreover, Wong does not teach any modulation capability.

Claim 15 further defines the method of claim 14, wherein the phase error trajectory is good when the change in the signal is less than a specified threshold. Claim 15 is allowable for the same reasons set forth above in support of the allowance of Claim 14.

Claim 16 further defines the method of claim 14, wherein the measuring the change in the signal comprises measuring a peak, a variance, or a rate of change in the signal. Claim 16 is allowable for the same reasons set forth above in support of the allowance of Claim 14.

Claim 17 further defines the method of claim 1, wherein the test is for frequency lock and the signal is the output of a phase detector, and wherein the manipulation comprises comparing a value of the signal over several samples. Claim 17 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 19 further defines the method of claim 17, wherein the samples are taken at different times. Claim 19 is allowable for the same reasons set forth above in support of the allowance of Claim 17.

Claim 20 further defines the method of claim 1, wherein the test is for frequency deviation and the signal is an output of an integral accumulator of a loop filter, and wherein the manipulation comprises comparing the signal with a specified range. Claim 20 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 21 further defines the method of claim 20, wherein the frequency deviation is within acceptable limits when the signal is within the specified range. Claim 21 is allowable for the same reasons set forth above in support of the allowance of Claim 20.

Claim 22 further defines the method of claim 20, wherein the manipulation further comprises comparing several samples of the signal. Claim 22 is allowable for the same reasons set forth above in support of the allowance of Claim 20.

Claim 24 further defines the method of claim 1, wherein the RF circuit contains an all-digital phase-locked loop, and the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth. Claim 24 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 27 further defines the method of claim 1, wherein the RF circuit is an all-digital frequency synthesizer. Claim 27 is allowable for the same reasons set forth above in support of the allowance of Claim 1.

Claim 28 further defines the method of claim 1, wherein the RF circuit is an all-digital transmitter. Claim 28 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Moreover, Wong does not teach any transmitter.

Claim 29 further defines the method of claim 28, wherein the transmitter is used in a wireless communications network. Claim 29 is allowable for the same reasons set forth above in support of the allowance of Claim 28.

Claim 30 further defines the method of claim 29, wherein the wireless communications network is Bluetooth compliant. Claim 30 is allowable for the same reasons set forth above in support of the allowance of Claim 29.

Claim 31 further defines the method of claim 1, wherein the testing comprises a functional test or a compliance test of the RF circuit. Claim 31 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Further, Wong does not teach any compliance testing.

Claim 43 further defines the circuit of claim 41 further comprising a loop filter coupled to the phase detector and the DCO, the loop filter to provide a desired amount of attenuation to the computed difference between the reference phase and the variable phase. Claim 43 is allowable for the same reasons set forth above in support of the allowance of Claim 41. Examiner's determination seems to be supposition not supported by fact since Examiner does not offer any explanation or further details. Consequently, the combining of references as suggested by the Examiner would not work and the claim rejection is improper.

Claim 45 further defines the circuit of claim 44, wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a parallel fashion. Claim 45 is allowable for the same reasons set forth above in support of the allowance of Claim 44. Further, Examiner has provided no reasoning for the rejection of this claim. Accordingly, no prima facie case of obviousness of claim 45 has been established. The 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 46 further defines the circuit of claim 44, wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a cascaded fashion. Claim 46 is allowable for the same reasons set forth above in support of the allowance of Claim 44. Further, Examiner has provided no reasoning for the rejection of this claim. Accordingly, no prima facie case of obviousness of claim 46 has been established. The 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

13) Claim 24 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Wong et al. (US 5,295,079), as applied to claim 1 above, and further in view of Skierszkan et al. (US Publication 2002/0001359 A1). Applicants respectfully traverse this rejection as set forth below.

Claim 24 further defines the method of claim 1, wherein the RF circuit contains an all-digital phase-locked loop, and the method further comprises prior to the observing, setting the all-digital phase-locked loop to a certain bandwidth. Claim 24 is allowable for the same reasons set forth above in support of the allowance of Claim 1. Moreover, Applicants respectfully traverse Examiner's determination: "Skierszkan discloses an acquisition PLL that has a low pass filter with a relatively high cut-off frequency. The acquisition PLL tracks all changes in the input signal, including error components." In actuality, the "acquisition PLL" is a separate PLL and adding a new PLL to the DPLL in Girardeau would not work since having two PLL's would bring issues of their differing performances, such as jitter or drift. The two PLL's would have separate oscillators and each oscillator is independent. Since the topic of Girardeau's invention is testing, now Girardeau's tests would need to be duplicated without solving the fundamental issue of setting *the* PLL into different bandwidth. Accordingly, Examiner's combination of Girardeau, Wong and Skierszkan and corresponding rejection of Claim 24 is improper and must be withdrawn.

14) Claim 45 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Wong et al. (US 5,295,079), as applied to claims 1 and 41 above, and further in view of Ko et al. (US 5,982,832). Applicants respectfully traverse this rejection as set forth below.

Claim 45 further defines the circuit of claim 44, wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a parallel

fashion. Claim 45 is allowable for the same reasons set forth above in support of the allowance of Claim 44. Moreover, Figure 4 in Ko does not show "a plurality of filters arranged in a parallel fashion", as suggested by Examiner. The cited text describes the structure filters as n filters with the phase detector selecting one filter among the n filters. In addition, combining Ko into Girardeau would not work since the output of such a filer could not be connected to the oscillator 23. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

15) Claim 46 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Wong et al. (US 5,295,079), as applied to claims 1 and 41 above, and further in view of Cucchietti et al. (US 4,819,080). Applicants respectfully traverse this rejection as set forth below.

16) Claim 46 further defines the circuit of claim 44, wherein the loop filter is comprised of a plurality of filters, and wherein the filters are arranged in a cascaded fashion. Claim 45 is allowable for the same reasons set forth above in support of the allowance of Claim 44. Moreover, Combining Cucchiett into Girardeau would not work since the output of such a filer could not be connected to the oscillator 23. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

17) Claim 2 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Wong et al. (US 5,295,079), as applied to claim 1 above, and further in view of Kim et al. (US 6,885,700). Applicants respectfully traverse this rejection as set forth below.

Claim 2 further defines the method of claim 1, wherein the testing is performed using built-in self test (BIST) techniques. Claim 45 is allowable for the same reasons set forth above in support of the allowance of Claim 44. Furthermore, the combination of Girardeau, Wong and Kim does not satisfy the limitation "wherein the **testing** is performed", which is positively recited and required by Claim 2. Girardeau does not teach or even suggest testing and incorporating Wong and Kim will change nothing in this regard.

Combining Kim into Girardeau does not make sense because the objective of the DPLL in Girardeau is not test or even built-in self-test (BIST) but the main or mission mode of its operation, which includes agility and being robust over the changing environment. Girardeau teaches an apparatus and method for determining a feedback divider ratio in a digital phase locked loop (DPLL) by monitoring the drift in the feedback signal. The drift could be caused by using an unknown frequency of fixed frequency system clock 22. (col. 2, lines 28-39). Hence monitoring the frequency drift of the external clock is not related to testing, so there is no motivation to incorporate Kim. Furthermore, the test or BIST would imply reporting back the results outside of the circuit. No such mechanism is reported in Girardeau simply because he does not teach the test or BIST. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

18) Claims 10 & 44 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Wong et al. (US 5,295,079), as applied to claim 1 above, and further in view of Mathe et al. (US 5,825,253). Applicants respectfully traverse this rejection as set forth below.

Claim 10 further defines the method of claim 8, wherein the all-digital phase-lock loop is operating in a type-I mode, and the signal is an output of an infinite impulse

response filter coupled to the output of a loop filter. Claim 10 is allowable for the same reasons set forth above in support of the allowance of Claim 8. Further, Mathe cannot be combined with Girardeau since operating on a 1-bit output of the phase detector by an IIR filter would change the signal nature (i.e., multi-bit) which will make the DPLL system inoperable. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 44 further defines the circuit of claim 43, wherein the loop filter is of a type selected from a group consisting of a finite impulse response filter, an infinite impulse response filter or combination thereof. Claim 44 is allowable for the same reasons set forth above in support of the allowance of Claim 43. Further, Mathe cannot be combined with Girardeau since operating on a 1-bit output of the phase detector by an FIR filter or IIR filter or a combination thereof would change the signal nature (i.e., multi-bit), which would not connect to the oscillator 23 (requires 1-bit RETARD/ADVANCE signals) and which will further make the DPLL system inoperable. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

19) Claims 12 & 47 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Wong et al. (US 5,295,079), as applied to claims 1 and 41 above, and further in view of Koshiro et al. (US 5,768,326). Applicants respectfully traverse this rejection as set forth below.

Claim 12 further defines the method of claim 6, wherein the signal is an output of a gain normalization block. Claim 12 is allowable for the same reasons set forth above in support of the allowance of Claim 6. Moreover, it is not possible to normalize the 1-bit output of the phase detector 30/32, which is equated by the Examiner to

"signal" in the present claim. Consequently, incorporating Koshiro into Girardeau does not make sense and would not possibly work.

Further, even if, arguendo, it were possible in Girardeau to normalize the phase detector output, doing so would not make much sense. The Digital Oscillator 23 is a purely digital circuit ("comprises a counter and a decoder"; col. 3, line 17) synchronously operating on Unknown System Clock 22 so its gain is known precisely. In contrast, the oscillator characteristics in the instant application are subject to process, voltage and temperature variations so normalizing the signal to the gain of the oscillator is beneficial. No such motivation exists in Girardeau. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 47 further defines the circuit of claim 41 further comprising a gain normalization unit coupled to the phase detector and the DCO, the gain normalization unit to normalize the difference between the reference phase and the variable phase with respect to a gain in the DCO. Claim 47 is allowable for the same reasons set forth above in support of the allowance of Claim 41. Moreover, it is not possible to normalize the 1-bit output of the phase detector 30/32, which is equated by the Examiner to "signal" in the present claim. Consequently, incorporating Koshiro into Girardeau does not make sense and would not possibly work.

Further, even if, arguendo, it were possible in Girardeau to normalize the phase detector output, doing so would not make much sense. The Digital Oscillator 23 is a purely digital circuit ("comprises a counter and a decoder"; col. 3, line 17) synchronously operating on Unknown System Clock 22 so its gain is known precisely. In contrast, the oscillator characteristics in the instant application are subject to process, voltage and temperature variations so normalizing the signal to the gain of the oscillator is beneficial. No such motivation exists in Girardeau. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

20) Claim 18 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Yamaguchi et al. (US 6,687,629 B1), as applied to claims 1 and 41 above, and further in view of Gustafson et al. (US 4,086,539). Applicants respectfully traverse this rejection as set forth below.

Claim 18 further defines the method of claim 17, wherein the frequency has been locked when a variance in the magnitude is less than a specified threshold. Claim 18 is allowable for the same reasons set forth above in support of the allowance of Claim 17. Further, it is not possible to compute variance of the 1-bit phase detector output in Girardeau. The phase detector output is a sign signal so computing variance of a sign would be meaningless. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

21) Claim 42 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Girardeau, Jr. (US 5,486,792) in view of Wong et al. (US 5,295,079), as applied to claim 41 above, and further in view of Knudsen et al. (US 7,079,611). Applicants respectfully traverse this rejection as set forth below.

Claim 42 further defines the circuit of claim 41 further comprising a time-to-digital converter (TDC) coupled to the DCO and the phase detector, the TDC containing circuitry to compute a time difference between a reference clock and a variable clock. Claim 42 is allowable for the same reasons set forth above in support of the allowance of Claim 41. Further, adding the teachings of Knudsen, which introduces a circuit to compute and digitize a time difference between clocks, to Girardeau does not seem to make any sense. Claim 42 is a dependent claim of Claim 41, not Claim 1. The Examiner has not shown how other elements of Claim 41 are equated with Girardeau. Accordingly, the 35 U.S.C. 103(a) rejection is improper and must be withdrawn.

Claim 26 further defines the method of claim 25, wherein the setting, observing, and manipulating is repeated for several different all-digital phase-locked loop bandwidths, and wherein the producing comprises subtracting the calculated mean square errors for the several different all-digital phase-lock loop bandwidths. Examiner has provided no rejection for this claim. Accordingly, Claim 26 stands allowable.

Claim 27 further defines the method of claim 1, wherein the RF circuit is an all-digital frequency synthesizer. Examiner has provided no rejection for this claim. Accordingly, Claim 27 stands allowable.

Claims 1-3 and 5-47 stand allowable over the cited art for the reasons set forth above. New claims 48-54 stand similarly allowable. Applicants respectfully request allowance of the application as the earliest possible date.

Respectfully submitted,

/Ronald O. Neerings/
Reg. No. 34,227
Attorney for Applicants

TEXAS INSTRUMENTS INCORPORATED
P.O. BOX 655474, M/S 3999
Dallas, Texas 75265
Phone: 972/917-5299
Fax: 972/917-4418